faces in a transition region from the cell field to the edge region are avoided by varying the compensation in the transition region.

8. The semiconductor device of claim **5**, wherein there is a variable degree of compensation, in the difference between the p- and n-dopant dosages, between an almost fully compensated state in the cell field to a reduction in the p-dopant dosages towards the edge region.

9. The semiconductor device of claim **5**, wherein the semiconductor body in the edge region opposite the capacitance-increasing field plate includes a highly doped, n^+-conducting zone.

10. The semiconductor device of claim **5**, wherein the cell field towards the edge region includes charge compensation zones which decrease in width towards the edge region at constant stepwidth.

11. The semiconductor device of claim **5**, wherein the cell field towards the edge region includes charge compensation zones which decrease in depth towards the edge region at constant stepwidth.

12. The semiconductor device of claim **5**, wherein the semiconductor body includes a voltage-receiving zone at the transition from the cell field to the edge region in which the field plate has a recess which reduces voltage spikes, thereby avoiding sharp curves in equipotential surfaces, the field plate regions before and after the recess being electrically connected to the gate bond contact area.

13. A process for producing a semiconductor device with a charge carrier compensation structure comprising:

completing of drift zones and charge compensation zones on the semiconductor body which takes the form of a semiconductor wafer and the application of a gate oxide in the cell field;

applying of a field plate oxide layer thicker than the gate oxide in the edge region;

applying of an electrically conductive, capacitance-increasing field plate structure on the field plate insulating layer simultaneously with the application of gate electrode material in the cell field;

applying of an intermediate insulating layer in the edge region of the capacitance-increasing field plate structure simultaneously with the application of an intermediate insulating layer in the cell field and the opening of through-plated holes to the field plate structure in the intermediate insulating layer; and

applying of electrically conductive bond contact areas in the edge region forming a bond with the capacitance-increasing field plate structure.

14. The process of claim **13**, wherein the capacitance-increasing field plate is positioned beneath a gate bond contact area and set to gate potential by contact vias through an intermediate insulating layer.

15. The process of claim **13**, wherein the capacitance-increasing field plate is positioned beneath a source bond contact area and set to source potential by contact vias through an intermediate insulating layer.

16. The process of claim **13**, wherein the capacitance-increasing field plate is electrically connected to near-edge planar or trench gate electrodes of the cell field and to a gate bond contact area.

17. The process of claim **13**, wherein a highly doped n^+-conducting zone is inserted into the semiconductor body in the edge region opposite the capacitance-increasing field plate by ion implantation and/or diffusion.

18. The process of claim **13**, wherein sharp radii of curvature of the equipotential lines/equipotential surfaces in a transition region from the cell field to the edge region are avoided by varying the compensation in the transition region.

19. The process of claim **13**, wherein a variable degree of compensation, i.e. the difference between the p- and n-doping dosages, from the almost fully compensated status in the cell field to a reduction of the p-doping dosages towards the edge region is used.

20. The process of claim **13**, wherein charge compensation zones provided with decreasing width towards the edge region at constant stepwidth are applied towards the edge region of the semiconductor body.

21. The process of claim **13**, wherein charge compensation zones provided with decreasing depth towards the edge region at constant stepwidth are applied towards the edge region of the semiconductor body.

22. The process of claim **13**, wherein a voltage-receiving zone is provided in the edge region at the transition from the cell field to the edge region, and the field plate in the voltage-receiving zone being provided with a recess which reduces sharp curves of equipotential surfaces.

23. The process of claim **13**, wherein a field plate insulating layer thicker than the gate oxide and thinner than subsequent intermediate insulating layers is applied in the edge region by using the thermal oxidation of the silicon semiconductor body and/or by using the depositing of an insulating material.

24. The process of claim **13**, wherein the application of an electrically conductive, capacitance-increasing field plate structure on the field plate oxide layer takes place simultaneously with the application of gate electrode material in the cell field by the depositing and structuring of a highly doped polysilicon.

25. The process of claim **13**, wherein the application of an intermediate insulating layer in the edge region on the capacitance-increasing field plate structure takes place simultaneously with the application of an intermediate insulating layer in the cell region by using the depositing and structuring of silicon oxide or silicon nitride.

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